To clarify the record, Applicants point out that the Applicants' Attorney did not request claim 11 to be included in Group II. It was the Examiner who made the request. Applicants' Attorney merely gave consent, on behalf of the Applicant, as a courtesy to the Examiner.

Claim Objections

Paragraph 1 of the Office Action objects to claim 28 because it is missing. The Office Action states that correction and renumbering of all elected claims is required.

Applicants request, pursuant to MPEP 2266 and 37 C.F.R. 1.111, that this objection be held in abeyance until the finding of allowable subject matter. This is an objection as to form and as such, is not necessary to further consideration of the claims.

Claim Amendments

Claims 1, 2, 4, 5, 7, 8, 17-19 and 29 have been amended to more particularly point out and distinctly claim the inventions recited by these claims. Claim 30 has been amended to correct a minor typographical error. The specification provides support for the amendments to claims 1, 2, 4, 5, 7, 8, at least, for example, at one or more portions of page 14 lines 29-30; page 17, lines 6-21; page 18 lines 15-19; page 19, lines 5-7; and/or page 27, line 14-page 28, line 30. The specification provides support for the amendment to claim 29 at least for example, at one or more portions of page 12 line 8-page 28, line 30. No new matter has been added.

New Claims

Claims 32-41 have been added. The specification provides support for the new claims at least for example, at one or more portions of page 12 line 8-page 28, line 30. No new matter has been added.

Rejections of Claims 1-9, 27 and 30 Under 35 U.S.C. 103

In paragraph 3, the Office Action rejects claims 1-9, 27 and 30 under 35 U.S.C. 103(a) as being unpatentable over Yamashita (U.S. Patent No. 5,890,432) in view of Dingwall et al. (U.S. Patent No. 5,332,997).

The Office Action states that Yamashita shows (citing FIG. 4) a handset that includes a digital to analog converter 307, and that Dingwall discloses a switched capacitor DAC network

comprising a plurality of DACs 11 (citing FIG. 6) each of which comprises a plurality of capacitors that share charge with one another (citing FIG. 2).

The Office Action further states that Yamashita does not show a switched capacitor network having a plurality of DACs as recited in claims 1-9, 27, 30, but that it would have been obvious to utilize the switched capacitor DAC network in FIGS. 2, 6 of Dingwall for the DAC 307 in FIG. 4 of Yamashita, for the purpose of loading data at a high speed (citing col. 3, lines 29-35 of Dingwall et al., " ... due to the small gate capacitance of the switching transistors the loading of the data onto their gates is accomplished very quickly ...").

I. Applicants traverse the rejections of claims 1-9, 27 and 30 on the grounds that the proposed combination is improper.

As further discussed below, the proposed combination is improper for at least the following reasons: (1) the references teach away from the proposed combination, (2) the proposed combination would leave the circuit of Yamashita inoperative, and (3) even if the proposed combination would be operational, the Office Action has not presented legally sufficient evidence to support the proposed motivation, which is in fact illusory.

Yamashita discloses a handset in which speech signals are received from a microphone 106, coded by a speech CODEC 304 and a channel CODEC 305, and then modulated by a MODEM 306 to produces modulated in-phase (I) and quadrature-phase (Q) transmitting signals. A DAC 307 converts the modulated in-phase (I) and quadrature-phase (Q) transmitting signals to analog transmitting signals TxDI and TxDQ, respectively, that are transferred to the RF transmitter 202 of the system. (column 5, lines 34-40).

Dingwall discloses (in FIG. 6), a serial data generator with 40 output data word lines (DWL1 through DWL40). Each output data word line carries 144 bits of serial information which are distributed onto 24 sublines. Each subline carries 6 digital data bits to a corresponding serial-input, binary weighted DAC 11, which converts the 6 serial data bits into an analog signal (col. 5, lines 5-15). The DAC 11 uses a binary weighted capacitive network 50, which is comprised of binary-weighted storage capacitors (FIG. 2, col. 5, lines 58-65).

First, observe that Dingwall itself teaches away from the proposed combination. Dingwall states that there are "*problems*" with the DAC shown in FIGS. 2, 6 (see col. 12, lines 15-22). Dingwall states that the binary weighted capacitive network used in the DAC of FIGS. 2, 6 and shown in FIG. 2, requires "*very large*" or "*very small*" capacitors (col. 12, lines 15-22)

(emphasis added). The very small capacitors are "*difficult to make accurately*" and there is the "*additional problem*" of stray capacitance (col. 12, lines 22-24) (emphasis added). On the other hand, large capacitors take "*too much space*" (col. 12, lines 23-25) (emphasis added). The "*problem becomes worse*" when more than 6 binary steps are desired (col. 12, lines 21-22) (emphasis added). Dingwall suggests that the problems "may be alleviated" by adding additional circuitry; however, in view of all of these problems, why would anyone skilled in the art even consider using the DAC of Dingwall in the handset of Yamashita? He all but expressly says not to!

Second, the proposed combination would leave the circuit in Yamashita *inoperative*. The DAC 11 in Dingwall is a serial-input DAC. In contrast thereto, the DAC 307 of Yamashita is coupled to a channel coder 305 (which typically produce a parallel output), therefore suggesting that it is a parallel-input DAC (extra circuitry would be needed if the DAC 307 were not a parallel-input DAC). A serial-input DAC is not interchangeable with a parallel-input DAC, and therefore, cannot be substituted for the parallel-input DAC 307 of Yamashita, without leaving the circuit inoperative, a result that clearly makes the proposed combination improper. MPEP 2143.01 states that the proposed modification cannot render the prior art unsatisfactory for its intended purpose. Further, even if the circuit of Yamashita could be further modified (by adding additional circuitry not proposed by the Office Action) so as to operate with the DAC of Dingwall, such modifications have not been proposed by the Office Action, and the potential impact to size, cost, power, performance, etc., clearly teaches away from any attempts to do so.

The Office Action states that one skilled in the art would carry out the proposed modification for the purpose of loading data at a high speed (citing col. 3, lines 29-35 of Dingwall et al.). This proposed motivation is illusory. First, one skilled in the art would not make a modification that would leave the circuit unusable for its intended purpose. Second, even if the proposed combination were operational, the Office Action has not presented legally sufficient evidence to support the proposed motivation.

To try to satisfy the Office's burden of proof as to motivation, the Office Action cites a statement from Dingwall to the effect that data is loaded very quickly onto the gates of the switching transistors. The Office Action thus implies that one skilled in the art would make the modification to improve speed. However, the "evidence" set forth by the Office Action merely implies that the DAC in Dingwall may be faster than other *Dingwall-type* DACs. This says absolutely nothing about whether there is a speed advantage to putting the DAC of Dingwall into

Yamashita, and is thus irrelevant. If speed is the concern, then the issue is not whether the DAC of Dingwall is faster than other Dingwall type DAC's, but rather, the speed of the serial-input DAC in Dingwall compared to the speed of the parallel-input DAC in Yamashita. Yet the evidence set forth by the Office Action does not say anything about the speed of the DAC in Dingwall versus the DAC in Yamashita. Consequently, there is no support for the contention that the proposed combination, even if operational, would be expected to produce a speed improvement in Yamashita. Thus, the burden of proof as to motivation is not met.

Moreover, because the DAC of Dingwall is a serial-input DAC and the DAC in Yamashita would appear to be a parallel-input DAC, it is likely that the DAC of Dingwall is actually *slower*, not faster, than the DAC in Yamashita, thereby actually teaching *away* from the proposed combination.

Consequently, the proposed combination is improper and neither Yamashita, nor Dingwall nor any legally tenable combination thereof, teaches or suggests the inventions recited in claims 1-9, 27 and 30.

Claims 1-9, 27 and 30 should now be allowed.

Claims 2-3 and 35-38 depend from claim 1 and are patentable for at least the same reasons as stated above for claims 1. Reconsideration and allowance of claims 2-3 and 35-38 is respectfully requested. Claims 5-6 and 8-9 depend from claims 4 and 7, respectively, and are patentable for at least the same reasons as stated above for claims 4 and 7. Reconsideration and allowance of claims 5-6 and 8-9 is respectfully requested.

II. Neither Yamashita, nor Dingwall nor any proposed combination thereof teaches or suggests or makes obvious the inventions recited claims 1-9 and 30.

Claims 1-9

Claim 1, as amended, recites a system comprising "a DAC that receives a multi-bit digital signal and outputs at least two analog signals including a first analog signal and a second analog signal, the first analog signal being indicative of a sum of values of bits in the multi-bit digital signal, the second analog signal *also being indicative of said sum of value*s of said bits in the multi-bit digital signal." (emphasis added).

Neither Yamashita, nor Dingwall nor any proposed combination thereof teaches a DAC that outputs a "first analog signal being indicative of a sum of values of bits" and a "second

analog signal *also being indicative of said sum of values* of said bits", as recited in claim 1 (emphasis added).

Dingwall teaches that each of the DACs 11 receives its *own* serial data bits and outputs one analog signal indicative of a sum of values of those bits.

Yamashita teaches that the DAC 307 converts the modulated in-phase (I) and quadrature-phase (Q) transmitting signals to analog transmitting signals TxDI and TxDQ, respectively.

Therefore, neither Yamashita, nor Dingwall nor any proposed combination thereof teaches or suggests or makes obvious a system comprising "a DAC that receives a multi-bit digital signal and outputs at least two analog signals including a first analog signal and a second analog signal, the first analog signal being indicative of a sum of values of bits in the multi-bit digital signal, the second analog signal *also being indicative of said sum of values* of said bits in the multi-bit digital signal", as recited in claim 1 (emphasis added).

Accordingly, claim 1, and claims 2-3, 35-38 depending therefrom, should now be allowed.

Claim 4, as amended, recites a method comprising: "receiving a multi-bit digital signal; and generating at least two analog signals including *a first* analog signal that is indicative of a sum of values of bits in the multi-bit digital signal, *and a second* analog signal that is *indicative of said sum of values* of said bits in the multi-bit digital signal." (emphasis added).

Neither Yamashita, nor Dingwall, nor any proposed combination thereof, teaches or suggests or makes obvious generating "*a first* analog signal that is indicative of a sum of values of bits" and "*a second* analog signal that is *indicative of said sum of values* of said bits", as recited in claim 4 (emphasis added).

Accordingly, claim 4, and claims 5-6 depending therefrom, should now be allowed.

Claim 7, as amended, recites a system comprising: "means for receiving a multi-bit digital signal; and means for generating at least two analog signals including *a first* analog signal that is indicative of a sum of values of bits in the multi-bit digital signal, *and a second* analog signal that is *indicative of said sum of values* of said bits in the multi-bit digital signal." (emphasis added).

Neither Yamashita, nor Dingwall, nor any proposed combination or modification thereof, teaches or suggests generating "*a first* analog signal that is indicative of a sum of values of bits" and "*a second* analog signal that is *indicative of said sum of values* of said bits", as recited in claim 7. (emphasis added).

Therefore, claim 7, and claims 8-9 depending therefrom, should now be allowed.

Claim 30

Claim 30, recites a digital to analog converter that "receives a first multi-bit digital signal and a second multi-bit digital signal ,and produces an analog output that is indicative of a *product* of the first multi-bit digital signal and the second multi-bit digital signal." (emphasis added).

Neither Yamashita, nor Dingwall, nor any proposed combination thereof, teaches or suggests a DAC that "produces an analog output that is indicative of a *product* of the first multi-bit digital signal and the second multi-bit digital signal", as recited in claim 30, (emphasis added).

Indeed, there does not appear to by any mention in either Yamashita or Dingwall of a product of a first multi-bit digital signal and a second multi-bit digital signal.

Note that the Office Action does not indicate how Yamashita, or Dingwall, or any combination thereof, could possible teach or suggest a DAC that produces an analog output that is indicative of a product of a first multi-bit digital signal and a second multi-bit digital signal, as recited in claim 30.

Consequently, neither Yamashita, nor Dingwall, nor any proposed combination thereof, teaches or suggests a digital to analog converter that "receives a first multi-bit digital signal and a second multi-bit digital signal ,and produces an analog output that is indicative of a *product* of the first multi-bit digital signal and the second multi-bit digital signal", as recited in claim 30, (emphasis added).

Accordingly, claim 30 should be allowed.

Note that because the reasons given herein are sufficient to traverse the rejections, Applicants do not address other possible reasons for traversing the rejections.

Rejections of Claims 16 and 29 Under 35 U.S.C. 103

In paragraph 4, the Office Action rejects claims 16 and 29 under 35 U.S.C. 103(a) as being unpatentable over Barrow et al. (U.S. Patent No. 5,036,322) in view of Dingwall et al. (U.S. Patent No. 5,332,987).

The Office Action states that Barrow et al discloses (in FIG. 2) a binary weighted DAC 38 and a segmented DAC 36. The Office Action further states that Barrow does not show the

detail structure of the segmented DAC as recited in claims 16 and 29, but that it would have been obvious to utilize the switched capacitor D/A converter network in FIGS. 2, 6 of Dingwall for the segmented DAC 36 in FIG. 2 of Barrow et al., for the purpose of loading data at a high speed (citing col. 3, lines 29-35 of Dingwall et al.).

I. Applicants traverse the rejections of claims 16 and 29 on the grounds that the proposed combination is improper.

As further discussed below, the proposed combination is improper for at least the following reasons: (1) the references teach away from the proposed combination, (2) the proposed combination would leave the circuit of Barrow inoperative, and (3) even if the proposed combination would be operational, the Office Action has not presented legally sufficient evidence to support the proposed motivation, which is in fact illusory.

Barrow et al. discloses high accuracy digital to analog converters (Abstract). FIG. 2 shows an embodiment of a DAC 20 that includes a parallel-input, segmented DAC 36 and a binary-weighted DAC 38.

Dingwall is described above.

First, observe that Dingwall itself teaches *away* from the proposed combination. Dingwall states that there are "*problems*" with the DAC shown in FIGS. 2, 6 (see col. 12, lines 15-22). Dingwall states that the binary weighted capacitive network used in the DAC of FIGS. 2, 6 and shown in FIG. 2, requires "*very large*" or "*very small*" capacitors (col. 12, lines 15-22) (emphasis added). The very small capacitors are "*difficult to make accurately*" and there is the "*additional problem*" of stray capacitance (col. 12, lines 22-24) (emphasis added). On the other hand, large capacitors take "*too much space*" (col. 12, lines 23-25) (emphasis added). The "*problem becomes worse*" when more than 6 binary steps are desired (col. 12, lines 21-22) (emphasis added). Dingwall suggests that the problems "may be alleviated" by adding additional circuitry; however, in view of all of these problems, why would anyone skilled in the art even consider using the DAC of Dingwall in the high accuracy converter of Barrow?

Second, the proposed combination would leave the circuit in Barrow inoperative. The DAC 36 in Barrow is a parallel-input, segmented DAC 36. The DAC 11 in Dingwall is a serial-input, binary weighted DAC. A serial-input, binary weighted DAC is not interchangeable with a parallel-input, segmented DAC, and therefore, cannot be substituted for the parallel-input, binary weighted DAC 307 of Barrow, without leaving the circuit inoperative, a result that clearly makes

the proposed combination improper. MPEP 2143.01 states that the proposed modification cannot render the prior art unsatisfactory for its intended purpose. Further, even if the circuit of Barrow could be further modified (by adding additional circuitry not proposed by the Office Action) so as to operate with the DAC of Dingwall, such modifications have not been proposed by the Office Action, and the potential impact to size, cost, power, performance, etc., clearly teaches away from any attempts to do so.

The Office Action states that one skilled in the art would carry out the proposed modification for the purpose of loading data at a high speed (citing col. 3, lines 29-35 of Dingwall et al.). This proposed motivation is illusory. First, one skilled in the art would not make a modification that would leave the circuit unusable for its intended purpose. Second, even if the proposed combination were operational, the Office Action has not presented legally sufficient evidence to support the proposed motivation.

To try to satisfy the Office's burden of proof as to motivation, the Office Action cites a statement from Dingwall to the effect that data is loaded very quickly onto the gates of the switching transistors. The Office Action thus implies that one skilled in the art would make the modification to improve speed. However, the "evidence" set forth by the Office Action merely implies that the DAC in Dingwall may be faster than other *Dingwall-type* DACs. This says absolutely nothing about whether there is a speed advantage to putting the DAC of Dingwall into Barrow, and is thus irrelevant. If speed is the concern, then the issue is not whether the DAC of Dingwall is faster than other *Dingwall-type* DAC's, but rather, how the speed of the serial-input DAC in Dingwall compares to the speed of the parallel-input DAC in Barrow. Yet the evidence set forth by the Office Action does not say anything about the speed of the serial-input DAC in Dingwall versus the parallel-input DAC in Barrow. Consequently, there is no support for the contention that the proposed combination, even if operational, would be expected to produce a speed improvement in Barrow. Thus, the burden of proof as to motivation is not met.

Moreover, because the DAC in Dingwall is a serial-input DAC and the DAC in Barrow et al. is a parallel-input DAC, it is likely that the DAC of Dingwall is actually *slower*, not faster, than the DAC in Barrow et al., thereby actually teaching *away* from the proposed combination.

Therefore, the proposed combination is improper and neither Barrow, nor Dingwall nor any legally tenable combination thereof, teaches or suggests the inventions recited in claims 16 and 29.

Accordingly, claims 16 and 29 should now be allowed.

Claims 17-21, 32 and 39-41 depend from claim 29 and are patentable for at least the same reasons as stated above for claim 29. Reconsideration and allowance of claims 17-21, 32 and 39-41 is hereby respectfully requested.

II. Neither Barrow, nor Dingwall nor any proposed combination thereof teaches or suggests or makes obvious the invention recited in claim 29.

Claim 29

Claim 29 recites a system comprising "a digital signal processing stage that receives a multi-bit input and provides a multi-bit output; and a switched capacitor DAC that receives a multi-bit input signal that includes the multi-bit output of the digital signal processing stage, the switched capacitor DAC having a plurality of sub DACs that each receive an associated amount of charge in response to the multi-bit input signal received by the DAC, the switched capacitor DAC having an operating state in which at least two of the plurality of sub DACs share charge with one another such that the associated charges are redistributed, and having an operating state in which the switched capacitor DAC outputs an analog signal that is indicative of the multi-bit input signal received by the switched capacitor DAC *using less than all of the redistributed charge*" (emphasis added).

Neither Barrow et al, nor Dingwall, nor any proposed combination thereof, teaches or suggests a switched capacitor DAC that redistributes charge and "outputs at least one analog signal indicative of the multi-bit input signal received by the DAC *using less than all of the redistributed charge*", as recited in claim 29 (emphasis added).

Consequently, neither Barrow et al, nor Dingwall, nor any proposed combination thereof, teaches or suggests a system comprising: "a digital signal processing stage that receives a multi-bit input and provides a multi-bit output; and a switched capacitor DAC that receives a multi-bit input signal that includes the multi-bit output of the digital signal processing stage, the switched capacitor DAC having a plurality of sub DACs that each receive an associated amount of charge in response to the multi-bit input signal received by the DAC, the switched capacitor DAC having an operating state in which at least two of the plurality of sub DACs share charge with one another such that the associated charges are redistributed, and having an operating state in which the switched capacitor DAC outputs an analog signal that is indicative of the multi-bit input signal received by the switched capacitor DAC *using less than all of the redistributed charge*", as recited in claim 29, (emphasis added).

Accordingly, claim 29, and claims 17-21, 32 and 39-41 depending therefrom, should now be allowed.

Note that because the reasons herein are sufficient to traverse the rejections, Applicants do not address other possible reasons for traversing the rejections.

Claim Rejections Under 35 U.S.C. 102

In paragraph 6, the Office Action rejects claim 17-24 under 35 U.S.C. 102(e) as being unpatentable over Watson et al. (U.S. Patent No. 6,154,162).

The Office Action states that Watson et al. discloses in Fig. 4, a system comprising a scrambler 42 and a switched capacitor DAC 42 having a plurality of capacitors 70, 72 and 74.

Applicants traverse the rejection.

Claims 17-21 have been amended to depend from claim 29 and are patentable for the reasons stated above.

Claim 22 recites "a digital to analog converter that receives a multi-bit digital signal and produces an analog output that is proportional to the *square* of the multi-bit digital signal." (emphasis added).

Watson does not teach or suggest a DAC that produces "an analog output that is proportional to the *square* of a multi-bit digital signal", as recited in claim 22 (emphasis added).

Neither does the Office Action state how Watson could possibly teach or suggest a DAC that produces an analog output that is proportional to the *square* of a multi-bit digital signal.

Accordingly, claim 22 should now be allowed.

Claims 23-24 depend from claim 22 and are patentable for at least the same reasons as stated above for claim 22. Reconsideration and allowance of claims 23-24 is requested.

Discussion as to Allowability of New Claims

Claim 33 recites a system comprising "a digital signal processing stage that receives a multi-bit input and provides a multi-bit output; and a switched capacitor DAC wherein the DAC comprises a switched capacitor network that receives a multi-bit input that includes the multi-bit output from the digital signal processing stage, the switched capacitor network having a plurality of sub DACs that each receive an associated bit of the multi-bit digital signal, each of the plurality of sub DACs having an associated capacitance that receives an associated amount of charge in response to the associated bit, the DAC having an operating state in which at least two

of the plurality of sub DACs share charge with one another, and having an operating state in which *less than all of the plurality of sub DACs are connected to an output terminal* and the switched capacitor network outputs at least one analog signal indicative of a sum of values of bits in the multi-bit input received by the DAC." (emphasis added).

Neither Yamashita, nor Dingwall, nor any proposed combination thereof, teaches or suggests a DAC inter alia "having an operating state in which *less than all of the plurality of sub DACs are connected to an output terminal* and the switched capacitor network outputs at least one analog signal indicative of a sum of values of bits in the multi-bit input received by the DAC", as recited in claim 33 (emphasis added).

Nor does Barrow et al, or Dingwall, or any proposed combination thereof, teach or suggest the DAC recited in claim 33.

Accordingly, allowance of claim 33 is requested.

Claim 34 depends from claim 33 and is patentable for at least the same reasons as stated above for claim 33. Reconsideration and allowance of claims 34 is hereby respectfully requested.

Provisional Double Patenting Rejections

Paragraph 8 of the Office Action states that claims 1-9 and 30 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting over claims 1-17 of co-pending Application No. 09/575,561. The Office Action states that although the conflicting claims are not identical, they are not patentably distinct from each other because all means as recited in claims 1-9 and 30 of the present application are seen to be included in rewording a rearranging claims 1-17 of the co-pending application.

Applicants note that these rejections are provisional and therefore do not require a response at this time. However, Applicants expressly reserve the right to respond at a future time.

Paragraph 9 of the Office Action states that claims 1-9 and 30 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting over claims 1-39 of co-pending Application No. 09/575,562. The Office Action states that although the conflicting claims are not identical, they are not patentably distinct from each other because the switched capacitor DAC as recited in claims 1-9 and 30 are read on the switched capacitor DAC network as recited in claims 1-39 of the co-pending application.

Applicants note that these rejections are provisional and therefore do not require a response at this time. However, Applicants expressly reserve the right to respond at a future time.

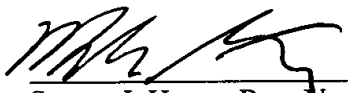
CONCLUSION

In view of the foregoing amendments and remarks, this application should now be in condition for allowance. A notice to this effect is respectfully requested. If the Examiner believes, after this amendment, that the application is not in condition for allowance, the Examiner is requested to call the Applicant's attorney at the telephone number listed below.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted

Ferguson, et al, Applicant

By: 

Steven J. Henry, Reg. No. 27,900
Mark Steinberg, Reg. No. 40,829
Wolf, Greenfield & Sacks, P.C.
600 Atlantic Avenue
Boston, Massachusetts 02210-2211
Tel. No.: (617) 720-3500
Attorney for Applicant

Docket No. A0312/7409/SJH/MXS
Date: March 25, 2002
x03/25/02x

MARKED-UP CLAIMS

1. (Amended) A system comprising:

a DAC that receives a multi-bit digital signal and outputs at least two analog signals [each] including a first analog signal and a second analog signal, the first analog signal being indicative of a sum of values of bits in the multi-bit digital signal, the second analog signal also being indicative of said sum of values of said bits in the multi-bit digital signal.

2. (Amended) The system of claim 1 wherein the [at least two analog signals] first analog signal and the second analog signal are substantially equal to each other.

4. (Amended) A method comprising:

receiving a multi-bit digital signal; and

generating at least two analog [output] signals [each] including a first analog signal that is indicative of a sum of values of bits in the multi-bit digital signal, and a second analog signal that is indicative of said sum of values of said bits in the multi-bit digital signal.

5. (Amended) The method of claim 4 wherein [generating comprises generating at least analog output signals that] the first analog signal and the second analog signal are substantially equal to one another.

7. (Amended) A system comprising:

means for receiving a multi-bit digital signal; and

means for generating at least two analog [output] signals [each] including a first analog signal that is indicative of a sum of values of bits in the multi-bit digital signal, and a second analog signal that is indicative of said sum of values of said bits in the multi-bit digital signal.

8. (Amended) The system of claim 7 wherein the [means for generating comprises means for generating at least two analog output signals that] first analog signal and the second analog signal are substantially equal to one another.

17. (Amended) [A] The system [comprising:] of claim 29 wherein the digital signal processing stage comprises

a scrambler [that receives input and provides output; and

and a switched capacitor DAC that has a plurality of capacitors and redistributes charge between at least two of the plurality of capacitors, coupled to the scrambler, that receives digital output of the scrambler].

18. (Amended) A system as claimed in claim 17 wherein [the scrambler comprises a plurality of outputs,] the number of bits in the multi-bit input to the DAC [comprises a plurality of inputs] is greater than the number of bits in the multi-bit output [outputs] of the scrambler.

19. (Amended) The system of claim 18 wherein at least one of the bits of the multi-bit input [inputs] to the scrambler is coupled to a first logic signal, and at least one of the bits of the multi-bit input [inputs] to the DAC is coupled to a second logic signal having a logic state opposite a logic state of the first signal.

29. (Amended) A system comprising:

a digital signal processing stage that receives a multi-bit input and provides a multi-bit output; and

a switched capacitor DAC that receives a multi-bit input signal that includes the multi-bit output of the digital signal processing stage, the switched capacitor DAC [has] having a plurality of [capacitors] sub DACs that each receive an associated amount of charge in response to the multi-bit input signal received by the DAC, the switched capacitor DAC having an operating state in which [and redistributes charge between] at least two of the plurality of [capacitors]sub DACs share charge with one another such that the associated charges are redistributed, [coupled to the digital signal processing stage, that receives digital output of the digital signal processing stage] and having an operating state in which the switched capacitor DAC outputs an analog signal that is indicative of the multi-bit input signal received by the switched capacitor DAC using less than all of the redistributed charge.

30. (Amended) A digital to analog converter receives a first multi-bit digital signal and a second multi-bit digital signal ,and produces an analog output that is indicative of a product of the first multi-bit digital signal and the second multi-bit digital signal.